IN THE CLAIMS

1. (Original) A behavior processor system for operating a portion of a user design and interfacing with a host testbench process, comprising:

a reprogrammable logic element for modeling a hardware model of the portion of the user design that includes a behavior level function; and

a testbench call back process for responding to the behavior level function in the reprogrammable logic element by sending a signal to the host testbench process.

2. (Original) The system of claim 1, wherein the behavior level function includes a condition.

3. (Previously Presented The system of claim 2, wherein the behavior level function includes a condition and the occurrence of the condition triggers the testbench call back process.

4. (Original) The system of claim 2, wherein the condition includes an "if-then" conditional statement implemented in hardware.

5. (Original) The system of claim 1, wherein the signal includes an interrupt from the testbench call back process to the host testbench process.

6. (Original) The system of claim 1, wherein the signal includes an interrupt from the reprogrammable logic element to the host testbench process.

7. (Original) The system of claim 1, wherein the signal includes data from the testbench call back process to the host testbench process.

8. (Previously Presented) The system of claim 1, wherein a reprogrammable logic element temporarily suspends operation upon the occurrence of the condition.

9. (Original) The system of claim 8, wherein the reprogrammable logic element resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host testbench process.

10. (Original) The system of claim 2, wherein the reprogrammable logic element temporarily pauses operation upon the occurrence of the condition.

11. (Original) The system of claim 1, wherein the reprogrammable logic element includes a clock that controls the speed of processing instructions and data in the reprogrammable logic element.

12. (Original) The system of claim 11, wherein the clock runs at 20 MHz.

13. (Original) A verification system for analyzing a user design, comprising:

a host workstation for modeling and operating a software model of the user design;

a reprogrammable hardware emulator for modeling a first hardware model of at least a portion of the user design; and

a behavior processor for modeling a second hardware model of a selected portion of the user design.

14. (Original) The verification system of claim 13, wherein the selected portion includes a behavioral aspect of the user design.

15. (Original) The verification system of claim 13, wherein the selected portion includes at least one condition in the user design.

16. (Original) The verification system of claim 15, wherein the at least one condition includes an "if- then" conditional statement.

17. (Original) The verification system of claim 13, wherein the behavior processor includes a testbench callback process for responding to the selected portion of the user design modeled in the reprogrammable hardware emulator by sending a signal to the host workstation.

18. (Previously Presented) The verification system of claim 13, wherein the selected portion includes at least one condition in the user design and the behavior processor includes a testbench callback process for responding to the at least one occurrence of the condition in the reprogrammable hardware emulator by sending a signal to the host workstation.

19. (Original) The verification system of claim 18, wherein the reprogrammable hardware emulator temporarily suspends operation upon the occurrence of the condition.

20. (Original) The verification system of claim 19, wherein the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended upon the service of the signal by the host workstation.

21. (Original) The verification system of claim 18, wherein the reprogrammable hardware emulator temporarily pauses operation upon the occurrence of the condition.

22. (Previously Presented) The verification system of claim 13, wherein the selected portion includes at least one condition for the user design and the behavior processor sends a wait signal to the reprogrammable hardware emulator upon the at least one occurrence of the condition so that the reprogrammable hardware emulator temporarily suspends operation.

23. (Original) The verification system of claim 22, wherein the behavior processor sends a resume signal to the reprogrammable hardware emulator upon the service of the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended.

24. (Original) The verification system of claim 22, wherein the behavior processor toggles the wait signal to the reprogrammable hardware emulator upon the service of the signal by the host workstation so that the reprogrammable hardware emulator resumes operation from the point at which operation was temporarily suspended.

25. (Original) The verification system of claim 13, wherein the behavior processor operates when it receives a request for service from the host workstation.

26. (Original) The verification system of claim 13, wherein the behavior processor operates when it receives a request for service from the reprogrammable hardware emulator.

27. (Currently Amended) A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:

modeling a behavioral portion of the user design in hardware, where the behavioral portion includes a service request; and

sending a signal to the testbench process in the host workstation upon the occurrence of the service request.

28. (Original) The method of claim 27, further comprising step:

suspending the operation of the simulation until the host workstation services the signal.

29. (Original) The method of claim 27, further comprising step:

suspending the operation of the simulation until the testbench process services the signal.

30. (Original) The method of claim 27, wherein the step of modeling the behavioral portion includes modeling conditional statements.

31. (Previously Presented) The method of claim 30, wherein the step of modeling the conditional statements includes "if-then" statements.

32. (Original) A method of verifying a user design where the verification environment includes a host workstation for running a simulation of the user design and a testbench process, comprising steps:

modeling a conditional portion of the user design in a hardware environment;

executing the conditional portion in the hardware environment; and

sending an interrupt to the testbench process in the host upon the occurrence of at least one condition in the conditional portion.

33. (Original) The method of claim 32, further comprising step:

suspending the operation of the simulation until the host workstation services the interrupt.

34. (Original) The method of claim 32, further comprising step:

suspending the operation of the simulation until the testbench process services the interrupt.

35. (Previously Presented) The method of claim 32, wherein the step of modeling the conditional portion includes "if-then" statements.

36. (Original) The method of claim 32, wherein the step of executing occurs at the

speed of a hardware clock.

37. (Original) The method of claim 36, wherein the step of executing occurs at 20 MHz.